WHAT IS CLAIMED IS:

1. A system comprising:

a first data processor having an input data port, and an output control port;

a memory having a data port to provide output data;

a first bit access controller having an input data port coupled to the output data port of the memory, an input control port coupled to the output control port and an output data port coupled to the input data port of the first data processor, the first bit manipulator further including:

a plurality of storage locations coupled to the input data port of the first bit manipulator, wherein each storage location stores data having N bit locations including a first bit and a last bit; and

a bit shift module having an input port coupled to the plurality of line storage locations, and an output port coupled to the input data port of the first data processor, the shifter to provide at its output shifted bit values that are shifted relative to their storage location within the plurality of line storage locations, wherein the shifted bit values are shifted based on a value received at the input control port.

2. The system of claim 1 wherein the plurality of storage locations are part of a circular buffer.

3. The system of claim 2, wherein the circular buffer is used to form a first in first out buffer.

4. The system of claim 1, wherein the plurality of storage locations are part of a first in first out buffer.

5. The system of claim 1 further comprising a memory control portion having a first control port coupled to a control port of the bit manipulator, and a second control port coupled to a control port of the memory, wherein the memory control portion requests data from memory to be stored in the plurality of storage locations.

6. The system of claim 5 further comprising a watermark storage location to store a value to indicate the memory control portion is to request data from memory.

7. The system of claim 1 wherein the first data processor further comprises a general purpose processor.

8. The system of claim 7, wherein the general data processor includes a RISC type processor.

9. The system of claim 8, wherein the RISC type processor includes a MIPs based processor.

10. The system of claim 9 further comprising a video processor, wherein the video processor is separate from the first data processor.

11. The system of claim 9, wherein the video processor includes a video transcoder.

12. The system of claim 1 further comprising a storage location coupled to the first bit access controller to store a value indicating an amount of valid data stored in the plurality of storage locations.

13. The system of claim 1, wherein the first bit access controller further includes a interrupt output coupled to an input of the first data processor, where the interrupt output is to be asserted by the first bit access controller each time a predetermined number of storage locations of the plurality of storage locations is accessed.

14. The system of claim 13, wherein the storage location is accessed when it is loaded with data.

15. The system of claim 13, wherein the storage location is accessed when its data is read.

16. A method comprising the steps of:

loading a plurality of data words into a storage location based upon a data request by a data processor;

when in a first mode of operation receiving an indicator from the data processor to implement a get_bits request; providing data from the storage location in response receiving the indicator from the data processor.

17. The method of claim 16, wherein the step of providing further includes implementing the get_bits in hardware.

18. The method of claim 16, wherein the step of providing further includes user selectively implementing one of one-filling and zero filling.

19. The method of claim 16, further comprising the step of:

when in a second mode of operation the indicator from the data processor is to implement a Huffman decode.

20. A method of using a general purpose data processor to access a portion of data bits of a plurality of data bits, the method comprising the steps of:

providing a first request for N data bits to a bit controller, the bit controller being separate from the general purpose data processor, where the first bit of the N data bits is not aligned on a byte boundary;

receiving the N data bits from the bit controller;

determining at the general purpose data processor if M data bits are available from the bit controller;

when the M data bits are available from the controller providing a second request for M data bits to the bit controller.

21. The method of claim 20 wherein the step of determining includes accessing a register associated with the bit controller to determine if M data bits are available.

22. The method of claim 20 further comprising the steps of:

receiving an interrupt indicating an amount of data used by the bit controller;

modifying an indicator based upon the interrupt, wherein the indicator is used during the step of determining to determine if M data bits are available.